Amendments to the Specification:

Please replace the paragraph starting on page 2, line 17 with the following:

In general, the present invention describes a synchronous clock generator, which permits an input signal to be latched, when the input signal is stable. Stability may occur after the transient time required for the input signal to transition between high and low levels. The synchronous clock generator may include a delay lock loop circuit, which is referenced to an input clock signal, to delay the clock signal by a period and also produce a control signal. The control signal may be supplied to a delay circuit receiving an input clock signal that is complementary ~~complimentary~~ to the input clock signal. The delay circuit may be used to delay the complementary ~~complimentary~~ clock signal by a period that is substantially the same as the delay caused by the delay lock loop circuit. The delayed clock signals may then be used to latch an input signal into a latch circuit, which allows the signals to stabilize. The synchronous clock generator may reduce the amount of area occupied on an integrated circuit, and may also reduce power consumption. Moreover, the synchronous clock generator may minimize the number of electrical components to delay the clock signals. Hence, operating temperatures and process delays that affect the electrical components may also be reduced.

Please replace the paragraph starting on page 3, line 14 with the following:

The delayed complementary ~~complimentary~~ clock signals also permit data to be latched on a rising edge of one of the clock signals in a given period and then on a rising edge of the other clock signal in the next period. Hence, the synchronous clock generator may eliminate a dependency on the duty cycle of an input clock signal.

Please replace the paragraph starting on page 3, line 20 with the following:

Fig. 1 illustrates a simplified block diagram of an integrated circuit 1 including an input/output interface 9 and an integrated circuit core 10. Signals may be exchanged between the core 10 and the input/output interface 9 using channels 16 and 17. The integrated circuit 1 may receive an input signal 2 at the input/output interface 9. The input signal 2 may include a data signal (DATA) 12, a clock signal (CLOCK) 13, and a clock signal ($\overline{CLOCK}$) 14. The clock signals 13 and 14 may be complementary ~~complimentary~~. The input signal 2 may be transmitted onto distinct channels. The channels may include a data channel 5, a clock channel 7, and a clock channel 8.

Please replace the paragraph starting on page 7, line 18 with the following:

Fig. 5 is a timing diagram illustrating an example of phase delays produced by the synchronous clock generator 8. The clock signals 13 (CLOCK) and 14 ($\overline{CLOCK}$) may be complementary ~~complimentary~~ and may have substantially the same period (T). The data signal 12 (DATA) received on the

channel 5 may also have the same period as the signals 13 and 14. Fig. 5 also shows that the output signal 23 ($CLOCK_{Delay}$) and the output signal 24 ($\overline{CLOCK}_{Delay}$) may be delayed by a period (T_L) relative to the input clock signals 13 and 14. The delay permits the data signal 12 to be latched on a rising edge 79 of the clock signal 13 or the rising edge 80 of the clock signal 14 at a time (T_L), after the transient time (T_{trans}) of the signal 12.